REMARKS

By this Amendment, Applicant amends claims 1 and 2 to more appropriately define the invention. Applicant submits that no new matter is introduced by this amendment. Claims 1-21 and 24-47 remain pending, with claims 3-21 and 24-34 withdrawn from further consideration as directed to a nonelected invention.

In the Final Office Action ("OA"), the Examiner rejected claims 1, 2, 35-37, and 39-45 under 35 U.S.C. § 102(b) as being anticipated by Miyawaki et al., U.S. Patent No. 5,567,962 ("Miyawaki"); and rejected claim 38 under 35 U.S.C. § 103(a) as unpatentable over Miyawaki.

Applicant respectfully points out that in the Final Office Action the Examiner did not make any reference to new claims 46 and 47 presented in the Amendment filed December 10, 2003. Applicant therefore respectfully requests the Examiner's consideration of claims 46 and 47 in the next Office Action.

Applicant respectfully traverses the rejections for the reasons set forth below.

I. Response to Rejection Under 35 U.S.C. § 102(b)

The Examiner rejected claims 1, 2, 35-37, and 39-45 under 35 U.S.C. § 102(b) as being anticipated by Miyawaki. In response, Applicant respectfully submits that Miyawaki fails to anticipate claims 1, 2, 35-37, and 39-45 because Miyawaki fails to teach all the elements of these claims.

In order to properly anticipate Applicant's claimed invention under 35 U.S.C. § 102(b), each and every element of the claim in issue must be found, either expressly described or under principles of inherency, in a single prior art reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." M.P.E.P. § 2131, ed. 8, rev. 1 (Feb. 2003) (quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236 (Fed. Cir.

1989)). Finally, "[t]he elements must be arranged as required by the claim." M.P.E.P. § 2131 at p. 2100-70.

Claim 1 is directed to a semiconductor device comprising a combination of elements including, *inter alia*, "a gate electrode having a side-wall gate portion provided over a side surface of [a] convex semiconductor layer, the gate electrode applying an electric field effect to [a] channel region and [a] semiconductor region via a gate insulator, a thickness of the gate insulator being constant on an entire surface of the convex semiconductor layer and being approximately 2.5 nm, and the side-wall gate portion being offset with respect to a part of a lower portion of [a] source region and a part of a lower portion of [a] drain region" (emphasis added). Although different in scope, claim 2 is directed to a semiconductor device including similar recitations.

Miyawaki is directed to a semiconductor memory device. Miyawaki discloses that the device comprises a substrate 1012, a gate electrode 1023, an impurity region 1016, and a gate oxide film 1022. Miyawaki, Fig. 12. In contrast to claims 1 and 2, Miyawaki discloses that the thickness of gate oxide film 1022 in the part where region 1016 and gate electrode 1023 are opposed to each other is not constant, but increases in thickness. *See* Miyawaki, Figs. 12, 13. This occurs because of the formation method of Miyawaki. Miyawaki discloses that the element separation region is formed using the LOCOS method. *See* Miyawaki, Fig. 32. Consequently, a "Bird's beak" is formed in that part of gate oxide film 1022 where region 1016 and gate electrode 1023 are opposed to each other. Therefore, the thickness of gate oxide film 1022 is not constant. Rather, the gate insulator increases in thickness at the lower portion of the gate.

Thus, Miyawaki fails to teach at least "a thickness of the gate insulator being constant on an entire surface of the convex semiconductor layer and being approximately 2.5 nm."

Accordingly, Miyawaki does not anticipate claims 1 and 2. For at least this reason, claims 1 and 2 are allowable.

Claims 35-37, and 39-44 are allowable at least due to their dependence from allowable claim 1 and claim 45 is allowable at least due to its dependence from allowable claim 2.

Moreover, claim 43 recites, *inter alia*, "wherein the gate insulating film comprises an oxide including at least one of Ta, Sr, Al, Zr, Hf, La and Ti." Miyawaki fails to teach this claim element. *See, e.g.*, Miyawaki, col. 9, l. 40 to col. 10, l. 29. Thus, Miyawaki fails to anticipate claim 43. For at least this reason, claim 43 is allowable.

II. Response to Rejection Under 35 U.S.C. § 103(a)

The Examiner rejected claim 38 under 35 U.S.C. § 103(a) as unpatentable over Miyawaki. In response, Applicant respectfully submits that a *prima facie* case of obviousness has not been established for claim 38 because Miyawaki fails to teach or suggest all the elements of this claim.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim elements. Furthermore, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." M.P.E.P. § 2143.03 (quoting *In re Wilson*, 424 F.2d 1382, 1385 (C.C.P.A. 1970)). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Third, there must be a reasonable expectation of success. M.P.E.P. § 2143 at pp. 2100-122 to 127.

Claim 38 depends from claim 1 and thus incorporates the elements of that claim. As mentioned above, Miyawaki fails to teach or suggest at least "a gate electrode having a side-wall gate portion provided over a side surface of [a] convex semiconductor layer, the gate electrode

applying an electric field effect to [a] channel region and [a] semiconductor region via a gate insulator, a thickness of the gate insulator being constant on an entire surface of the convex semiconductor layer and being approximately 2.5 nm, and the side-wall gate portion being offset with respect to a part of a lower portion of [a] source region and a part of a lower portion of [a] drain region" as recited in claim 1 and incorporated in claim 38 (emphasis added). Thus, a *prima facie* case of obviousness has not been established because Miyawaki fails to teach or suggest all the elements of claim 38. For at least this reason, claim 38 is allowable.

Moreover, claim 38 recites, *inter alia*, "wherein a width of the convex semiconductor layer is smaller than 0.2 μm." Miyawaki also fails to teach or suggest at least this claim element. Accordingly, a *prima facie* case of obviousness has not been established for claim 38. For at least this reason, claim 38 is allowable.

The Examiner also alleged that "it would have been obvious to one of ordinary skill in the art to use or combine (teaching of second reference) in the range as claimed." (OA at ¶ 5.) However, the Examiner cited only one reference, Miyawaki. Thus, Applicant is unclear as to which second reference the Examiner is referring since the Examiner mentions only one reference. Accordingly, Applicant requests clarification from the Examiner.

III. Claims 46 and 47

As noted above, the Examiner did not address claims 46 and 47 in the outstanding Office Action. Claims 46 and 47 are allowable at least due to their dependence from allowable claim 2.

IV. Conclusion

In view of the foregoing, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: June 17, 2004

By: RWG for Rajeev Gupta #37,744
Rajeev Gupta
Reg. No. 55,873